

# design ideas

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## Oscillator meets three requirements

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**T**HREE COMMON REQUIREMENTS for a clock source are a wide frequency range, a variable duty cycle with independently adjustable  $T_{ON}$  and  $T_{OFF}$  times, and the ability to synchronize with an external signal. The gated oscillator in Figure 1 satisfies all three requirements using just one 74LS123 and a handful of passive components.

To analyze the circuit, first assume that the A input of one-shot  $IC_{1A}$  connects to ground. Then,  $IC_{1B}$ 's positive-going  $\overline{Q}$  output triggers the B input of  $IC_{1A}$ , whose negative-going Q output triggers the A input of  $IC_{1B}$ . This dc positive feedback ensures that the circuit always self-starts.

The time constant  $C_2 \times (R_2 + R_4)$  determines the width of  $T_{ON}$ , and  $C_1 \times (R_1 + R_3)$  determines the width of  $T_{OFF}$ . For the 74LS123, the values of the external components at  $R_{EXT}$  and  $C_{EXT}$  essentially define the output pulse width,  $t_W$ , according to

$$t_W = K \cdot R_{EXT} \cdot C_{EXT},$$

where  $k=0.45$  for  $C_{EXT} > 1000$  pF. Assuming that  $R_A = R_1 + R_3$  and  $R_B = R_2 + R_4$ , the period and the duty cycle are as follows, respectively:

$$T = K \cdot R_A \cdot C_1 + K \cdot R_B \cdot C_2;$$

$$\text{DUTY CYCLE} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{K \cdot R_B \cdot C_2}{K \cdot R_A \cdot C_1 + K \cdot R_B \cdot C_2} = \frac{R_B \cdot C_2}{R_A \cdot C_1 + R_B \cdot C_2}.$$

If  $C_1 = C_2$ , then

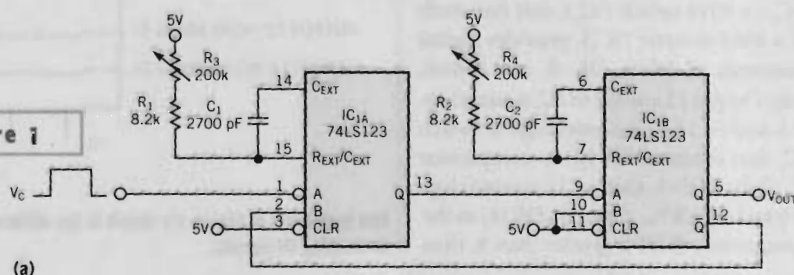
$$\text{DUTY CYCLE} = \frac{R_B}{R_A + R_B}.$$

The circuit oscillates at the frequency

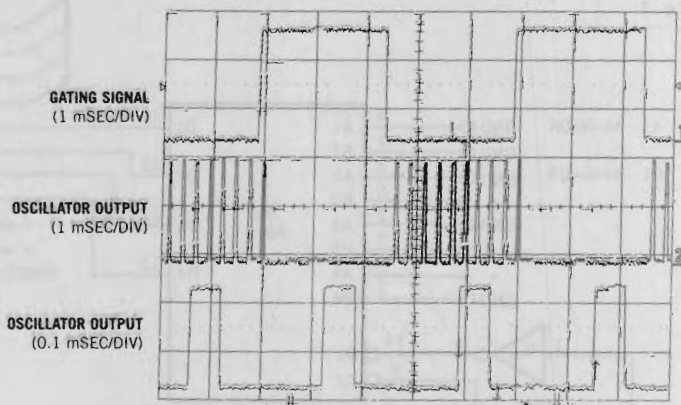
$$f = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{K \cdot R_A \cdot C_1 + K \cdot R_B \cdot C_2}.$$

Over the 74LS123's operating range,

Figure 1



(a)



(b)

NOTE:  
VERTICAL SCALE=200 mV/DIV.

A gated, astable oscillator (a) has an independently variable  $T_{ON}$  and  $T_{OFF}$ . The oscillator output is on when the gating signal is low (b).

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which is  $5\text{ k}\Omega \leq R_{\text{EXT}} \leq 200\text{ k}\Omega$  and assuming no limits for  $C_{\text{EXT}}$ , the duty cycle is 100% when  $R_A=5\text{ k}\Omega$  and  $R_B=200\text{ k}\Omega$ . The duty cycle is 0 when  $R_A=200\text{ k}\Omega$  and  $R_B=5\text{ k}\Omega$ . And, because  $T_{\text{ON}}$  and  $T_{\text{OFF}}$  are independent, you can vary the frequency without affecting the duty cycle.

You can easily turn the circuit into a

gated oscillator by applying a square-wave gating signal ( $V_C$ ) whose frequency is less than the oscillation frequency ( $f$ ) to the A input of  $IC_{1A}$ . The oscillator output is low when  $V_C$  is high and is free-running when the gating signal is low. In **Figure 1b**, the gating signal is 200 Hz,  $R_A=170\text{ k}\Omega$ ,  $R_B=50\text{ k}\Omega$ , and  $C_{\text{EXT}}=2700\text{ pF}$ . With these

values,  $T_{\text{ON}} \approx 60\text{ msec}$ ,  $T_{\text{OFF}} \approx 206\text{ msec}$ , and  $f \approx 3741\text{ Hz}$ . (DI #2276).

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## Simple circuit provides digital hysteresis

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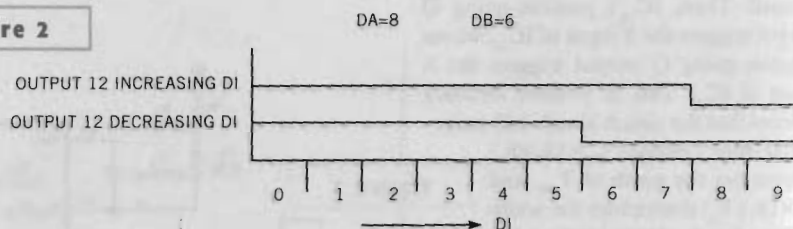
IT IS SOMETIMES USEFUL to have hysteresis in a digital circuit—for example, in a power circuit under the control of a manual pulse generator, in which mechanical vibrations can produce position errors. The circuit in **Figure 1**, which consists of a 4585 comparator ( $IC_2$ ), a 4019 switch ( $IC_1$ ), and one-sixth of a 4069 inverter ( $IC_3$ ), provides digital hysteresis. If  $DI=0$ ,  $DA=8$ , and  $DB=6$ , then Output 12 and G2 of  $IC_2$  assume logic 1, and G1 of  $IC_2$  assumes logic 0. Switch  $IC_1$  thus connects DA (8) to comparator  $IC_2$ . When  $DI=8$ , Output 12 assumes logic 0 and switch  $IC_1$  connects DB (6) to the comparator. If  $DI$  is greater than 8, then

Output 12 remains at logic 0. If  $DI$  becomes less than DB, then Output 12 assumes logic 1. **Figure 2** shows a pulse diagram. You can expand the circuit by adding more

comparators and switches. (DI #2274).

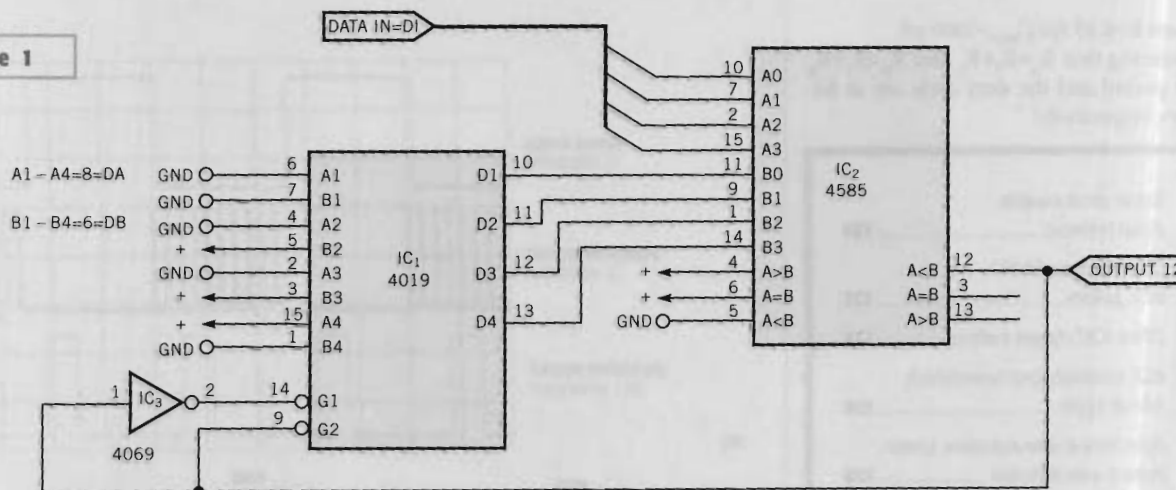
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**Figure 2**



The hysteresis in **Figure 1**'s circuit is the difference between the switching points for increasing and decreasing  $DI$  signals.

**Figure 1**



Digital hysteresis can provide a "debounce" function in digitally controlled switching circuits.